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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,032	09/11/2003	William Hugh Cochran	ROC920030125US1	5821

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Robert R. Williams
IBM Corporation - Dept. 917
3605 Highway 52 North
Rochester, MN 55901

EXAMINER	
RIZK, SAMIR WADIE	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 02/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/660,032	COCHRAN ET AL.	
	Examiner	Art Unit	
	Sam Rizk	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTIONS

- Claims 1-14 have been submitted for examination
- Claims 1-14 have been rejected

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Constantinescu US publication no. 2004/0252644 (Hereinafter Constantinescu) and further in view of Fred Schraff, Choosing Differential or single-ended measurements for data acquisition systems, Sensor Magazine Online, December 1997 (Hereinafter Schraff). Copy is provided in its entirety.

2. In Regard to claim 1, Constantinescu substantially teaches all the limitations:

- A method for implementing a redundancy enhanced differential signal interface comprising the steps of:

  (Note: Section [0021], line 4, in Constantinescu)

- detecting an error;

  (Note: Section [0021], lines (16-18) in Constantinescu)

- responsive to said detected error, reducing an interface operating speed,

  (Note: Section [0032], lines (6-10) in Constantinescu)

- alternately testing of true and complement sides of a differential signaling 1/0 pair; and

  (Note: Section [0032], lines (10-12) in Constantinescu)

However, Constantinescu does not disclose in detail:

- responsive to detecting a failure of a true side or a complement side, setting the detected failed true side or complement side to a reference voltage and maintaining said reduced interface operating speed.

Schraff, in an analogous art, that teaches reconfigurable Differential or single-ended measurements for data acquisition systems, disclose the method of:

- setting the detected failed true side or complement side to a reference voltage and maintaining said reduced interface operating speed.

  (Note: Figure 1, in Schraff)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Constantinescu with the teaching of Schraff to include implementation of dual single ended or differential interfaces responsive to detecting a failure.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized the need for interface redundancy mechanism where the interface degrades over time or quickly degrades while the interconnect is working within the system.

3. In regard to claim 2, Constantinescu teaches:

   - A method for implementing a redundancy enhanced differential signal interface as recited in claim 1 wherein the step of detecting said error includes the step of utilizing Error Correction Code (ECC) for error detecting.

     (Note: Section [0021], line 15, in Constantinescu)

4. In regard to claim 3, Constantinescu teaches:

   - A method for implementing a redundancy enhanced differential signal interface as recited in claim 1 wherein the step of reducing said interface operating speed includes the step of

setting an interface operating speed to about one half of normal operating speed.

(Note: Section [0032], line 8, in Constantinescu)

5. In regard to claim 4, Schraff teaches:

- A method for implementing a redundancy enhanced differential signal interface as recited in claim 1 wherein the step of alternately testing true and complement sides of a differential signaling 1/0 pair includes the steps of providing a pair of multiplexers coupled to a differential receiver, each multiplexer receiving a respective true or complement signal first input and a voltage reference second input; and each multiplexer providing a respective true or complement output signal to said differential receiver.

(Note: Figure 1, in Schraff)

6. Claim 5 is rejected for the same reasons as per claim 4.

7. In regard to claim 6, Constantinescu teaches:

- A method for implementing a redundancy enhanced differential signal interface as recited in claim 1 further includes the steps responsive to detecting a failure of both said true side and said complement side, returning to normal operating speed and posting said failure.

(Note: Section [0028], lines (16 and 17), in Constantinescu)

8. In regard to claim 7, Constantinescu teaches:

- A method for implementing a redundancy enhanced differential signal interface as recited in claim 1 further includes the steps responsive to detecting no failure of either a true side or a complement side, posting said detected no failure, and continuing operation at said reduced interface operating speed. (Note; FIG. 4, in Constantinescu)

9. In regard to claim 8, Constantinescu substantially teaches all the limitations:

- Apparatus for implementing a redundancy enhanced differential signal interface comprising:
  (Note: Section [0021], line 4, in Constantinescu)
- a differential signaling 1/0 pair;
  (Note: Section [0021], line 4, in Constantinescu)
- error detecting means coupled to said differential receiver for detecting an error;
  (Note: FIG. 4, reference character (404), in Constantinescu0
- test and failure control logic coupled to said error detecting means and said differential receiver interface; said test and failure control logic being responsive to a detected error, for reducing an interface operating speed', and alternately enabling said multiplexer control input of said pair of multiplexers for testing of true and complement sides of said differential signaling 1/0 pair; and responsive to detecting a failure of a true

side or a complement side, for setting the detected failed true side or complement side to a reference voltage for continued operation.

(Note: FIG. 4, reference characters (412), (414) and (416) in Constantinescu)

However, Constantinescu does not disclose in detail:

- a differential receiver interface coupled to said differential signaling 1/0 pair; said differential receiver interface including a pair of multiplexers coupled to a differential receiver, each multiplexer having a first input receiving a respective true or complement signal and a second input connected to a voltage reference and a multiplexer control input; and each multiplexer providing a respective true or complement output signal to said differential receiver;

Schraff, in an analogous art, that teaches reconfigurable Differential or single-ended measurements for data acquisition systems, disclose the method of multiplexers in Figures 1 and 6.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Constantinescu with the teaching of Schraff to include implementation of dual single ended or differential interfaces responsive to detecting a failure.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in

the art would have recognized the need for interface redundancy mechanism where the interface degrades over time or quickly degrades while the interconnect is working within the system.

10. In regard to claim 9, Constantinescu teaches:

- Apparatus for implementing a redundancy enhanced differential signal interface as recited in claim 8 wherein said test and failure control logic maintains said reduced interface operating speed for continued operation after setting the detected failed true side or complement side to a reference voltage.

  (Note: Section [0032], lines (6-10) in Constantinescu)

11. Claim 10 is rejected for the same reasons as per claim 6.

12. Claim 11 is rejected for the same reasons as per claim 7.

13. Claim 12 is rejected for the same reasons as per claim 3.

14. In regard to claim 13, Schraff teaches:

- Apparatus for implementing a redundancy enhanced differential signal interface a recited in claim 8 wherein said voltage reference is a middle level voltage between a high and low level of said differential signals.

  (Note: Figure 2, in Schraff)

15. Claim 14 is rejected for the same reasons as per claim 4.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Zhang et al. US patent no. 6601123 teaches method and apparatus to control the signal development rate of a differential bus.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Rizk whose telephone number is (571) 272-8191. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronics Business Center (EBC) at 866-217-9197 (toll-free)

Sam Rizk, MSEE, ABD

Examiner

ART UNIT 2133

1/30/06

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100